iCE40LM Family Data Sheet

Data Sheet

FPGA-DS-02043-1.9

July 2022

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DFF	D-style Flip-Flop
EBR	Embedded Block RAM
HFOSC	High Frequency Oscillator
I^2C	Inter-Integrated Circuit
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
NVCM	Non Volatile Configuration Memory
PFU	Programmable Functional Unit
PLB	Programmable Logic Blocks
PLL	Phase Locked Loops
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Packaging

1. General Description

iCE40LM™ is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40LM family includes integrated SPI and I²C blocks to interface with virtually all mobile sensors and application processors. The iCE40LM family also features two Strobe Generators that can generate strobes in microsecond ranges with the Low-Power Strobe Generator and in nanosecond ranges with the High-Speed Strobe Generator.

In addition, the iCE40LM family of devices includes logic to perform other functions such as mobile bridging, antenna tuning, GPIO expansion, motion/gesture recognition, IR remote control, bar code emulation, and other custom functions.

The iCE40LM family features three device densities, from 1100 to 3520 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I²C interface ports or general purpose I/Os. It also has up to 80 kbit of Block RAMs to work with user logic.

1.1. Features

- Flexible Logic Architecture
- Three devices with 1100 to 3520 LUTs
- 18 I/O pins for 25-pin WLCSP
- Ultra-low Power Devices
- Advanced 40 nm low power process
- As low as 120 µW standby power typical
- Embedded and Distributed Memory
- Two Hardened I²C Interfaces
- Two Hardened SPI Interfaces
- Two On-Chip Strobe Generators
- Low-Power Strobe Generator (Microsecond ranges)
- High-Speed Strobe Generator (Nanosecond ranges)
- High Current Drive Outputs for LED
- Three High Drive (HD) output in each device
- Source/sink nominal 24 mA
- Flexible On-Chip Clocking
- Six low-skew global signal resource
- Flexible Device Configuration
- SRAM is configured through SPI
- Ultra-Small Form Factor
- As small as 25-pin WLCSP package 1.71 mm × 1.71 mm
- Applications
- Smartphones
- Tablets and Consumer Handheld Devices
- Handheld Commercial and Industrial Devices
- Multi Sensor Management Applications
- Sensor Pre-processing and Sensor Fusion
- Always-On Sensor Applications

2. Product Family

Table 2.1 lists device information and packages of the iCE40LM family.

Table 2.1. iCE40LM Family Selection Guide

Part Number	iCE40LM1K	iCE40LM2K	iCE40LM4K
Logic Cells (LUT + Flip-Flop)	**1100**	**2048**	**3520**
RAM4K Memory Blocks	16	20	14
RAM4K RAM Bits	64 K	80 K	80 K
Package	**Programmable I/O Count**		
16-pin WLCSP, 1.71 mm x 1.71 mm, 0.35 mm	18	18	18
36-pin ucBGA, 2.5 mm x 2.5 mm, 0.40 mm	28	28	28
49-pin ucBGA, 3 mm x 3 mm, 0.40 mm	37	37	37

2.1. Overview

The iCE40LM family of ultra-low power FPGAs has three devices with densities ranging from 1100 to 3520 Look- Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), two Strobe Generators (LPSG, HSSG), two hardened I²C Controllers and two hardened SPI Controllers. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40LM devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as user configurable I²C and SPI Controllers, either as master or as slave, and two Strobe Generators.

The iCE40LM FPGAs are available in very small form factor packages, with the smallest in 25-pin WLCSP. The 25-pin WLCSP package has a 0.35 mm ball pitch, resulting to an overall package size of 1.71 mm x 1.71 mm that easily fits into a lot of mobile applications. Table 2.1 shows the LUT densities, package and I/O pin count.

The iCE40LM devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a *per-pin* basis.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40LM family of devices. Popular logic synthesis tools provide synthesis library support for iCE40LM. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40LM device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40LM FPGA family. Lattice also can provide fully verified bit-stream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. You can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's Reference Designs or fully-verified bitstreams, please contact your local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40LM family architecture contains an array of Programmable Logic Blocks (PLB), two Strobe Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40LM4K device.

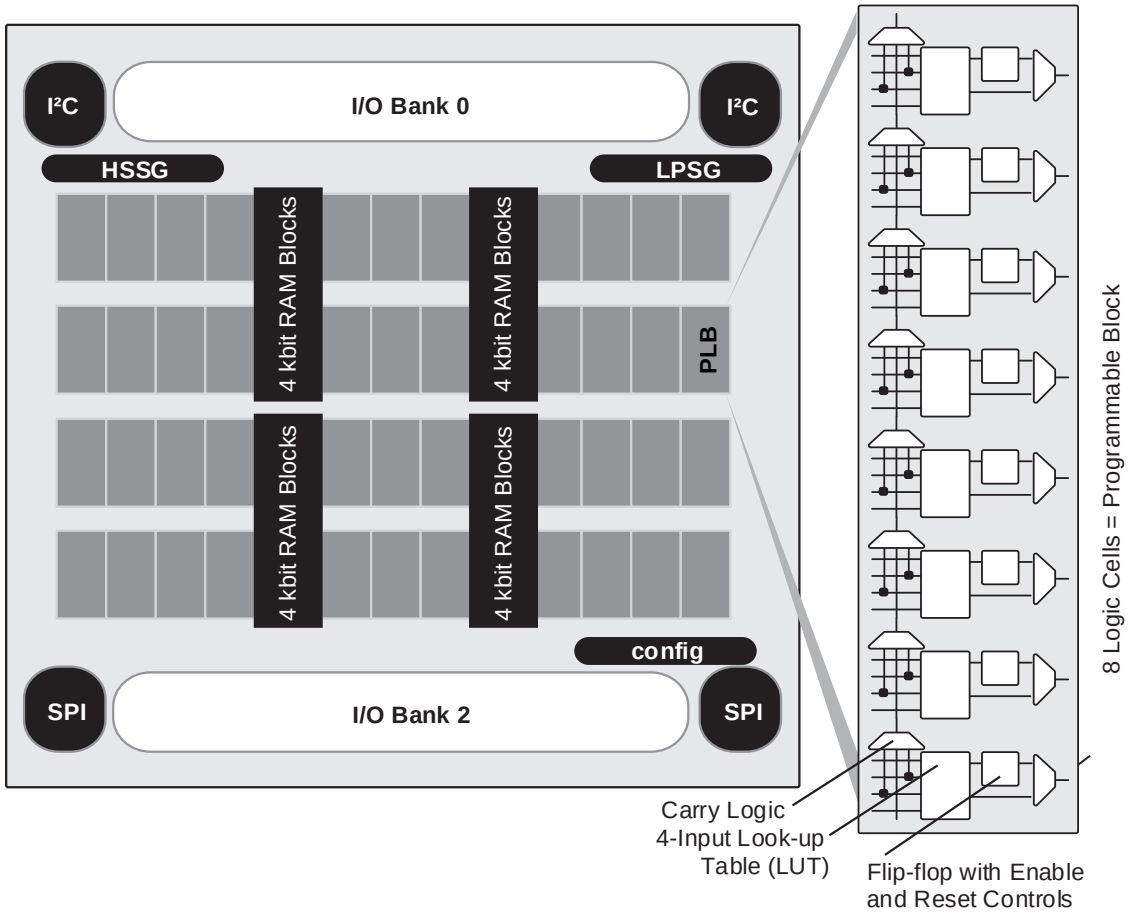


Figure 3.1. iCE40LM4K Device, Top View

The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40LM family, There are two sysI/O banks, one on top and one on bottom. You can connect both V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM, or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI ports also supports programming and configuration of the device. The iCE40LM also includes two user I²C ports, and two Strobe Generators.

3.1.1. PLB Blocks

The core of the iCE40LM device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 3.2. Each LC contains one LUT and one register.

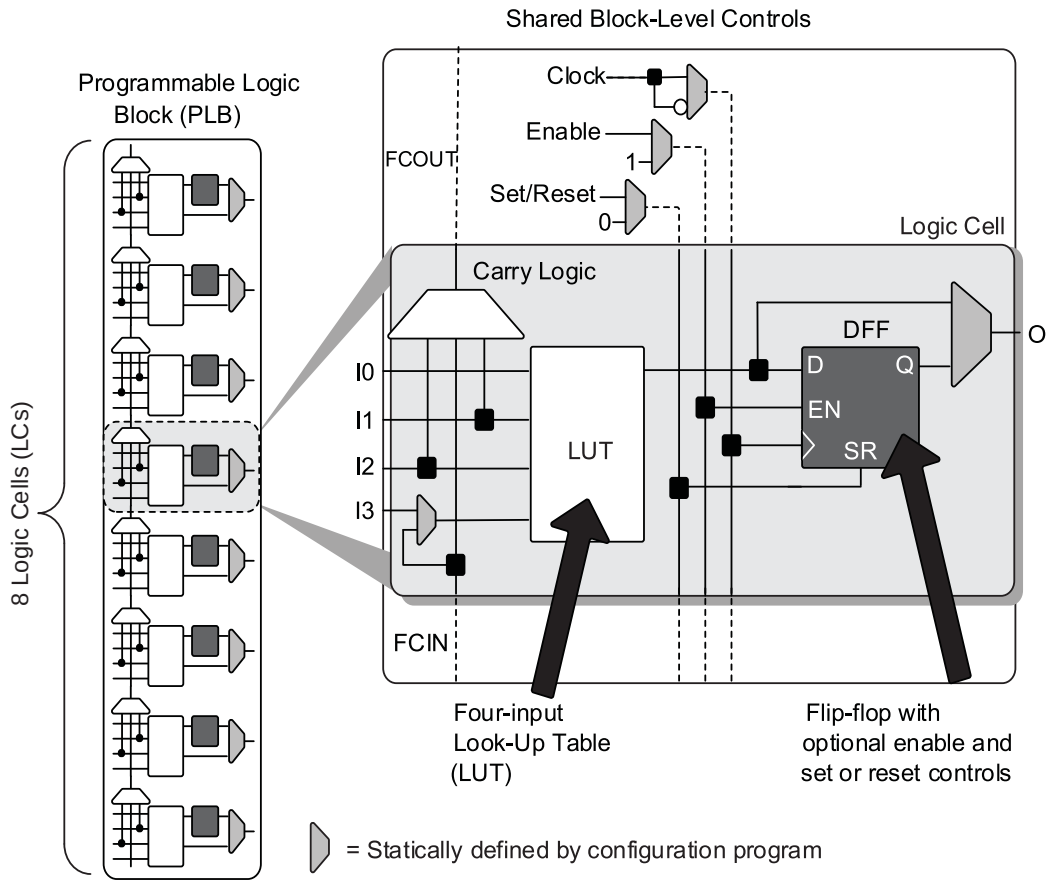


Figure 3.2. PLB Block Diagram

3.1.1.1. Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 3.2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A D-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 3.1 lists the logic cell signals.

Table 3.1. Logic Cell Signal Descriptions

Function	Type	Signal Name	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset*	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.

Function	Type	Signal Name	Description
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB.
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

***Note**: If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

3.1.2. Routing

There are many resources provided in the iCE40LM devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs), and x12 (spans thirteen PLBs). The adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal, and vertical directions.

The design tool takes the output of the synthesis tool, and places and routes the design.

3.1.3. Clock/Control Distribution Network

Each iCE40LM device has six global inputs, two pins on the top bank, and four pins on the bottom bank.

These global inputs can be used as high fanout nets, clock, reset, or enable signals. The dedicated global pins are identified as Gxx and the global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O, if they are not used to drive the clock nets.

Table 3.2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Strobe Generators (GBUF4 connects to LPSG, GBUF5 connects to HSSG).

Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	—
GBUF1		Yes	—	Yes
GBUF2		Yes	Yes	—
GBUF3		Yes	—	Yes
GBUF4		Yes	Yes	—
GBUF5		Yes	—	Yes
GBUF6		Yes	Yes	—
GBUF7		Yes	—	Yes

The maximum frequency for the global buffers are listed in Table 4.15.

3.1.3.1. Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40LM device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

3.1.3.2. Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40LM device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

3.1.4. sysCLOCK Phase Locked Loops (PLLs) (sysCLOCK PLL is only supported in 36-ball ucBGA package)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40LM devices have one sysCLOCK PLL (Please note that the 25-pin WLCSP package does not support the PLL). REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal strobe generator or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can either be programmed during configuration or adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

The iCE40LM PLL functions the same as the PLLs in the iCE40 family. For more details on the PLL, refer to iCE40 sysCLOCK PLL Design and Usage Guide.

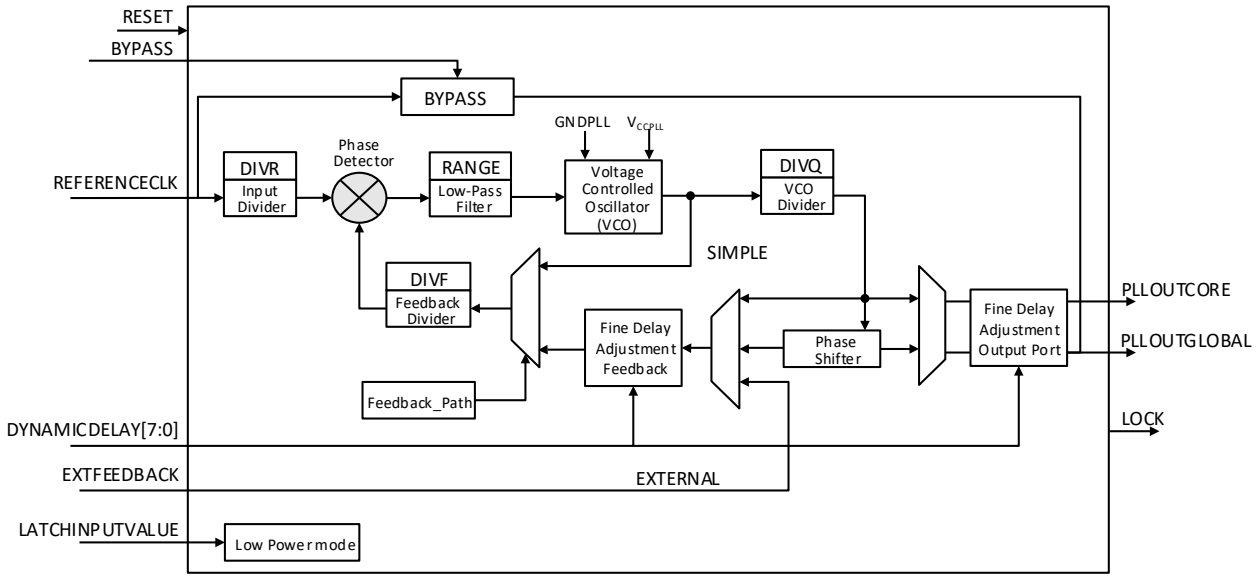


Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to 1 to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40LM device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

3.1.5.1. sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 3.4.

Table 3.4. sysMEM Block Configurations

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256 x 16 (4 K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512 x 8 (4 K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024 x 4 (4 K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048 x 2 (4 K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Note: For iCE40LM EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with an N and an R or W depending on the clock that is affected.

3.1.5.2. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

3.1.5.3. Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

3.1.5.4. RAM4K Block

Figure 3.4 shows the 256 x 16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

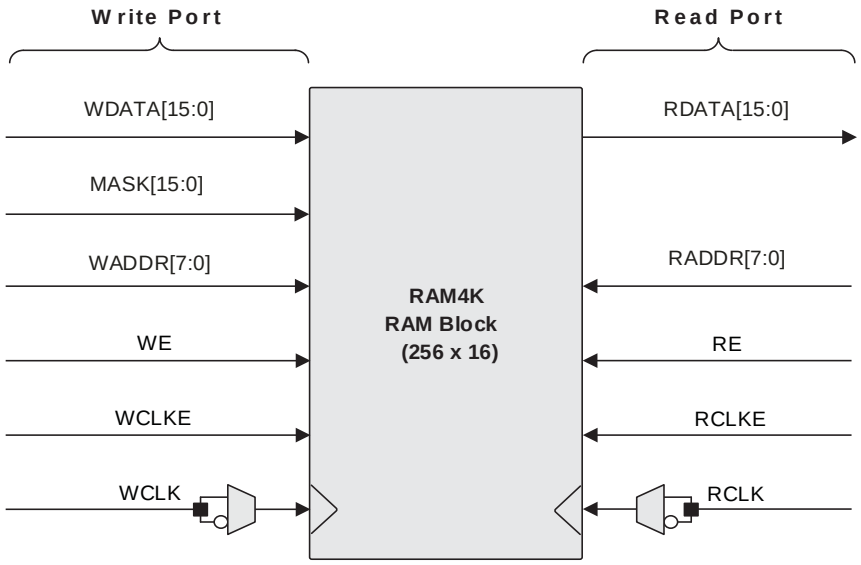


Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

The iCE40LM EBR block functions the same as EBR blocks in the iCE40 family. For further information, refer to Memory Usage Guide for iCE40 Devices (FPGA-TN-02002).

3.1.6. sysI/O Buffer Banks

iCE40LM devices have up to two I/O banks with independent V_{CCIO} rails. Configuration bank V_{CC_SPI} for the SPI I/Os is connected to V_{CCIO2} on the 25-pin WLCSP package.

3.1.6.1. Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysI/O buffers and pads. The PIOs are placed on the top and bottom of the devices.

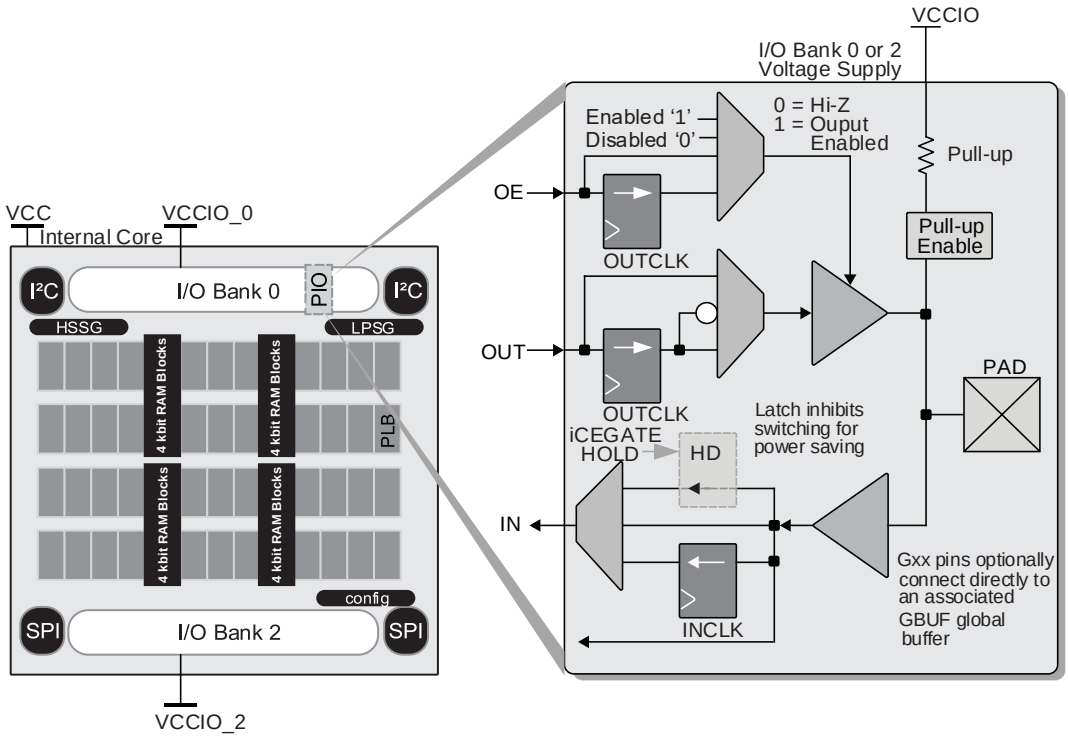


Figure 3.5. I/O Bank and Programmable I/O Cell

The PIO contains three blocks: an input register block, output register block iCEGate™, and tri-state register block. To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

3.1.6.2. Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

3.1.6.3. Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysI/O buffers.

Figure 3.6 shows the input/output register block for the PIOs.

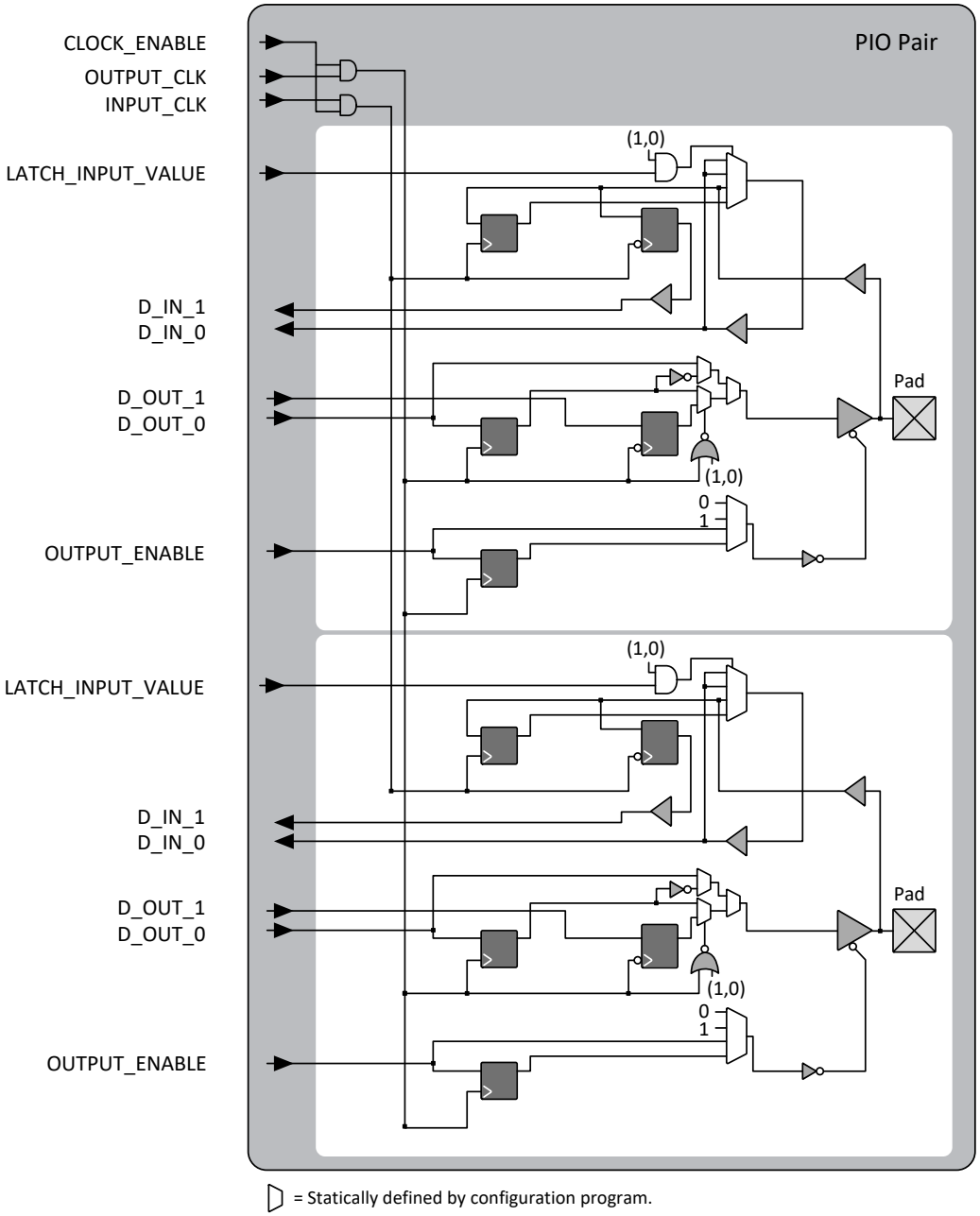


Figure 3.6. iCE40 I/O Register Block Diagram

Table 3.6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

3.1.7. sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow you to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

3.1.7.1. Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO_0}, V_{CCIO_2}, and V_{CC_SPI} (V_{CC_SPI} is connected to V_{CCIO_2} on the 25-pin WLCSP and 36-pin ucBGA packages) reach the level defined in Table 4.4. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC} and V_{CCIO_2} reach the defined levels. The I/Os take on the software user-configured settings only after V_{CC_SPI} reaches the level and the device performs a proper download/ configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

3.1.7.2. Supported Standards

The iCE40LM sysI/O buffer supports all single-ended input and output standards. The buffer supports the LVCMOS 1.8 V, 2.5 V, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 3.7 and Table 3.8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40LM devices.

Table 3.7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes	—	—
LVCMOS25	—	Yes	—
LVCMOS18*	—	—	Yes

Table 3.8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18*	1.8 V

3.1.8. On-Chip Strobe Generators

The iCE40LM devices feature two different Strobe Generators. One is tailored for low-power operation (Low Power Strobe Generator – LPSG), and generates periodic strobes in the microsecond (µs) ranges. The other is tailored for high-speed operation (High Speed Strobe Generator – HSSG), and generates periodic strobes in the Nanosecond (ns) ranges.

The Strobe Generators (HSSG and LPSG) provide fixed periodic strobes, and these strobes can be used as a clock source. When used as a clock source, the HSSG can provide strobe frequency in the range of 5 MHz - 20 MHz. The LPSG can provide strobe frequency in the range of 4 kHz - 20 kHz.

For further information on how to use the LPSG and HSSG, refer to iCE40LM On-Chip Strobe Generator Usage Guide (FPGA-TN-02212).

3.1.9. User I²C IP

The iCE40LM devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. Both I²C cores have preassigned pins, or you can select different pins, when the core is used.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support

For further information on the User I²C, refer to iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02010).

3.1.10. User SPI IP

The iCE40LM devices have two SPI IP cores. Both SPI cores have preassigned pins, or you can select different pins, when the SPI core is used. Both SPI IP core can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User I²C, refer to iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02010).

3.1.11. High Drive I/O Pins

The iCE40LM family devices offer 3 High Drive (HD) outputs in each device in the family. The HD outputs are ideal to drive LED signals on mobile application.

These HD outputs can be driven in different drive modes. The default is standard drive, which source/sink 8 mA current nominally. When HD drive option is selected, these HD outputs can source/sink 24 mA current nominally.

The pins on the HD I/Os are labeled with HD in it.

3.1.12. Power On Reset

iCE40LM devices have power-on reset circuitry to monitor V_{CC}, V_{CCIO_0}, V_{CCIO_2}, and V_{CC_SPI} voltage levels during power-up and operation. At power-up, the POR circuitry monitors these voltage levels. It then triggers download from the external Flash memory after reaching the power-up levels specified in Table 4.4. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

3.2. iCE40LM Configuration

This section describes the programming and configuration of the iCE40LM family.

3.2.1. Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From an SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40LM, refer to iCE40 Programming and Configuration (FPGA-TN-02001).

3.2.2. Power Saving Options

The iCE40LM devices feature iCEGate and PLL low power mode to allow you to meet the static and dynamic power requirements of their applications. Table 3.9 describes the function of these features.

Table 3.9. iCE40LM Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, it forces the PLL into low-power mode; PLL output is held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	–0.5	1.42	V
Output Supply Voltage V_{CCIO} and V_{CC_SPI}	–0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	–0.5	1.30	V
I/O Tri-state Voltage Applied	–0.5	3.60	V
Dedicated Input Voltage Applied	–0.5	3.60	V
Storage Temperature (Ambient)	–65	150	°C
Junction Temperature (T_J)	–65	125	°C

Notes:

- Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- Compliance with Thermal Management document is required.
- All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, V_{CCIO_2}	1.71	3.46	V
V_{CC_PLL}[4]	PLL Supply Voltage		1.14	1.26	V
V_{CC_SPI}[5]	Config SPI port Power Supply Voltage		1.71	3.46	V
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C

Notes:

1. Like power supplies must be tied together, V_{CCIO_0} to V_{CCIO_2}, if they are at same supply voltage and if they meet the power up sequence requirement. Please refer to Power Up Sequence section. V_{CC} and V_{CCPLL} are not recommended to be tied together. Refer to iCE40 Hardware Checklist (FPGA-TN-02006).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. For 25-pin WLCSP, PLL is not supported.
5. For 25-pin WLCSP and 36-pin ucBGA packages, V_{CC_SPI} is connected to V_{CCIO_2} on the package. V_{CC_SPI} is used to power the SPI1 ports in both configuration mode and user mode.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.01	10	V/ms

Notes:

- Assumes monotonic ramp rates.
- Power up sequence must be followed. See the Power-up Sequence section.

4.4. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels

Symbol	Parameter		Min	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (circuit monitoring V_{CC}, V_{CCIO_2}, and V_{CC_SPI})	V_{CC}	0.67	0.99	V
		V_{CCIO_2}, V_{CC_SPI}	0.70	1.59	V
V_{PORDN}	Power-On-Reset ramp down trip point (circuit monitoring V_{CC}, V_{CCIO_2}, and V_{CC_SPI})	V_{CC}	—	0.66	V
		V_{CCIO_2}, V_{CC_SPI}	—	1.59	V

Note: These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

4.5. Power-up Sequence

For all iCE40LM devices, it is required to have the V_{CC}/V_{CCPLL} power supply powered up before all other power supplies. The V_{CC}/V_{CCPLL} has to be higher than 0.5 V before other supplies are powered from GND.

In addition, for all iCE40LM devices, it is required that V_{CCSPI} not be the last power supply to ramp up. The V_{CCSPI} has to be higher than 0.5 V before the last supply is ramped.

In the required power up sequence, V_{CC}/V_{CCPLL} should be ramped first. Following V_{CC}/V_{CCPLL}, V_{CCSPI} should be ramped next, followed by the remaining supplies. On the 25-pin WLCSP, V_{CCPLL} is connected to V_{CC}, and is powered up together with V_{CC}. On the 25-pin WLCSP and 36-pin caBGA, V_{CCIO_2} is connected to V_{CC_SPI}, and should be powered up right after V_{CC}/V_{CCPLL} with V_{CCSPI}. Due to this connection, V_{CCIO_0} cannot connect to V_{CCIO_2} even if they are at the same supply voltage. The sequence is defined below:

- For 49-pin caBGA: V_{CC}, V_{CCPLL}, V_{CC_SPI}, V_{CCIO_0} and V_{CCIO_2}; Order of V_{CCIO_0} and V_{CCIO_2} is not important.
- For 36-pin caBGA: V_{CC}, V_{CCPLL}, V_{CC_SPI}/V_{CCIO_2}, V_{CCIO_0}
- For 25-pin WLCSP: V_{CC}/ V_{CCPLL}, V_{CC_SPI}/V_{CCIO_2}, V_{CCIO_0}

There is no power down sequence required. However, when partial power supplies are powered down, it is required that the above sequence is followed when these supplies are powered up again.

4.6. ESD Performance

Please contact Lattice Semiconductor for additional information.

4.7. DC Electrical Characteristics

Over recommended operating conditions.

Table 4.5. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	0 V < V_{IN} < V_{CCIO} + 0.2 V	—	—	±10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0 ≤ V_{IN} ≤ 0.65 V_{CCIO}	−3	—	−31	µA
		V_{CCIO} = 2.5 V, 0 ≤ V_{IN} ≤ 0.65 V_{CCIO}	−8	—	−72	µA
		V_{CCIO} = 3.3 V, 0 ≤ V_{IN} ≤ 0.65 V_{CCIO}	−11	—	−128	µA

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Refer to V_{IL} and V_{IH} in Table 4.10.
4. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.

4.8. Supply Current

Table 4.6. Supply Current[1, 2, 3, 4]

Symbol	Parameter	Typ VCC[4]	Unit
$I_{CCSTDBY}$	Core Power Supply Static Current	100	µA
$I_{CCPLLSTDBY}$	PLL Power Supply Static Current	11	µA
$I_{CCIOSTDBY}$, $I_{CC\_SPISTDBY}$	V_{CCIO}, V_{CC_SPI} Power Supply Static Current	2.5	µA
I_{CCPEAK}	Core Power Supply Startup Peak Current	11.2	mA
$I_{CCPLLPEAK}$	PLL Power Supply Startup Peak Current	2.8	mA
$I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$	V_{CCIO}, V_{CC_SPI} Power Supply Startup Peak Current	21.4	mA

Notes:

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. For 25-pin WLCSP, V_{CCPLL} is tied internally on the package, and V_{CC_SPI} is also connected to V_{CCIO_2} on the package..

4.9. User I²C Specifications

Table 4.7. User I²C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	µs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	µs
$t_{SU, DAT}$	Setup time (DATA)	250	—	—	100	—	—	µs
$t_{HD, DAT}$	Hold time (DATA)	0	—	—	0	—	—	µs
$t_{SU, STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	µs
$t_{HD, STA}$	Hold time (START condition)	4	—	—	0.6	—	—	µs
$t_{SU, STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	µs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	µs
$t_{CO, DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	µs

4.10. User SPI Specifications

Table 4.8. User SPI Specifications

Parameter Symbol	Parameter Description	Min	Typ	Max	Unit
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz
t_{HI}	HIGH period of SCK clock	9	—	—	ns
t_{LO}	LOW period of SCK clock	9	—	—	ns
$t_{SUmaster}$	Setup time (master mode)	2	—	—	ns
$t_{HOLDmaster}$	Hold time (master mode)	5	—	—	ns
$t_{SUslave}$	Setup time (slave mode)	2	—	—	ns
$t_{HOLDslave}$	Hold time (slave mode)	5	—	—	ns
$t_{SCK2OUT}$	SCK to out (slave mode)	—	—	13.5	ns

4.11. sysI/O Recommended Operating Conditions

Table 4.9. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min	Typ	Max
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

4.12. sysI/O Single-Ended DC Electrical Characteristics

Table 4.10. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}*		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} Max (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

***Note:** Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.

4.13. Typical Building Block Performance[1, 2]

4.13.1. Pin-to-Pin Performance (LVCMOS25)

Table 4.11. Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Unit
Basic Functions		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

4.13.2. Register-to-Register Performance

Table 4.12. Register-to-Register Performance

Function	Timing	Unit
Basic Functions		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
Embedded Memory Functions		
256 x 16 Pseudo-Dual Port RAM	150	MHz

Notes:

- The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
- Using a V_{CC} of 1.14 V at Junction Temp 85 °C.

4.14. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

4.15. Maximum sysI/O Buffer Performance

Table 4.13. Maximum sysI/O Buffer Performance

I/O Standard	Max Speed	Unit
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

Note: Measured with a toggling pattern.

4.16. iCE40LM Family Timing Adders

Over recommended commercial operating conditions.

Table 4.14. iCE40LM Family Timing Adders

Buffer Type	Description	Timing (Typ)	Unit
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	nS
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	MHz
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	MHz

Notes:

- Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
- LVCMOS timing measured with the load specified in Table 4.19.
- Commercial timing numbers are shown.

4.17. iCE40LM External Switching Characteristics

Over recommended commercial operating conditions.

Table 4.15. iCE40LM External Switching Characteristics

Parameter	Description	Device			Unit
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	650	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.1	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)*					
t_{SKEW_IO}	Data bus skew across a bank of I/Os	All devices	—	450	ps
t_{CO}	Clock to Output - PIO Output Register	All devices	—	11.5	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All devices	–0.23	—	ns
t_{H}	Clock to Data Holdp - PIO Input Register	All devices	5.55	—	ns

***Note:** 25-pin WLCSP package does not support PLL.

4.18. sysCLOCK PLL Timing – Preliminary

Over recommended operating conditions.

Table 4.16. sysCLOCK PLL Timing – Preliminary

Parameter	Description	Condition	Min	Max	Unit
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)	—	10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)	—	16	275	MHz
f_{VCO}	PLL VCO Frequency	—	533	1066	MHz
f_{PFD}	Phase Detector Input Frequency	—	10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	40	60	%
t_{PH}	Output Phase Accuracy	—	—	±12	deg
t_{OPJIT}[1, 5, 6]	Output Clock Period Jitter	f_{OUT} <= 100 MHz	—	450	ps p-p
		f_{OUT} > 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	f_{OUT} <= 100 MHz	—	750	ps p-p
		f_{OUT} > 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} <= 25 MHz	—	275	ps p-p
		f_{PFD} >c` 25 MHz	—	0.05	UIPP
t_{W}	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time	—	—	50	µs
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	f_{PFD} ≥ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{FDTAP}	Fine Delay adjustment, per Tap	—	98	226	ps
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable	—	—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width	—	100	—	ns

Parameter	Description	Condition	Min	Max	Unit
t_{RST}	RESET Pulse Width	—	10	—	ns
t_{RSTREC}	RESET Recovery Time	—	10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width	—	100	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time decreases to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values increase with loading of the PLD fabric and in the presence of SSO noise.
6. PLL jitter and lock time measurements are based on an external clean clock source. With different clock source, these values maybe different.

4.19. SPI Master Configuration Time

Table 4.17. SPI Master Configuration Time

Symbol	Parameter	Condition	Max	Unit
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	95	ms
		All devices – Medium frequency	35	ms
		All devices – High frequency	18	ms

Note: Assumes sysMEM Block is initialized to an all zero pattern, if they are used.

4.20. sysCONFIG Port Timing Specifications

Table 4.18. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge.	—	200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated.	—	49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40LM device is clearing its internal configuration memory.	—	1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read*	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH	—	20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW	—	20	—	—	ns
t_{STSU}	CCLK setup time	—	12	—	—	ns
t_{STH}	CCLK hold time	—	12	—	—	ns
t_{STCO}	CCLK falling edge to valid output	—	13	—	—	ns
Master SPI						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	6.5	—	13	MHz
		Medium Frequency	19.5	—	38	MHz
		High Frequency	33	—	66	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge	—	1200	—	—	µs

***Note:** Supported with 1.2 V Vcc and at 25 °C.

4.21. Switching Test Conditions

Figure 4.1 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.19.

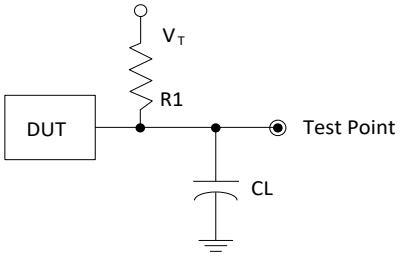


Figure 4.1. Output Test Load, LVCMOS Standards

Table 4.19. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L ≥ H, H ≥ L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z ≥ H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z ≥ L)			1.5 V	V_{OH}
Other LVCMOS (Z ≥ H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z ≥ L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H ≥ Z)			V_{OH} – 0.15 V	V_{OL}
LVCMOS (L ≥ Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

5. Pinout Information

5.1. Signal Descriptions

5.1.1. Power Supply Pins

Signal Name	Function	I/O	Description
V_{CC}	Power	—	Core Power Supply
V_{CCIO_0}, V_{CCIO_2}	Power	—	Power for I/Os in Bank 0 and 2.
V_{CC_SPI}	Power	—	Power supply for SPI1 ports. For 25-pin WLCSP and 36-pin ucBGA packages, this signal is connected to V_{CCIO_2}.
V_{CCPLL}	Power	—	Power supply for PLL. For 25-pin WLCSP, this is connected internally to V_{CC}.
GND/GNDPLL	GROUND	—	Ground

5.1.2. Configuration Pins

Signal Name	Function	I/O	Description
CRESET_B	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect a 10 kΩ pull-up to V_{CCIO_2}.
CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V_{CCIO2}.

5.1.3. Configuration SPI Pins

Signal Name		Function	I/O	Description
Primary	Secondary			
PIOB_xx[HD]	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O.
PIOB_xx[HD]	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O.
PIOB_xx[HD]	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as

Signal Name		Function	I/O	Description
Primary	Secondary			
				general I/O in user function [HD]=High Drive I/O.
PIOB_xx[HD]	SPI_SS	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function [HD]=High Drive I/O.

5.1.4. Global Signal Pins

Signal Name		Function	I/O	Description
Primary	Secondary			
PIOT_xx	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_xx	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOT_xx	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOT_xx	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOT_xx	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_xx	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.

5.1.5. LED Signal Pins

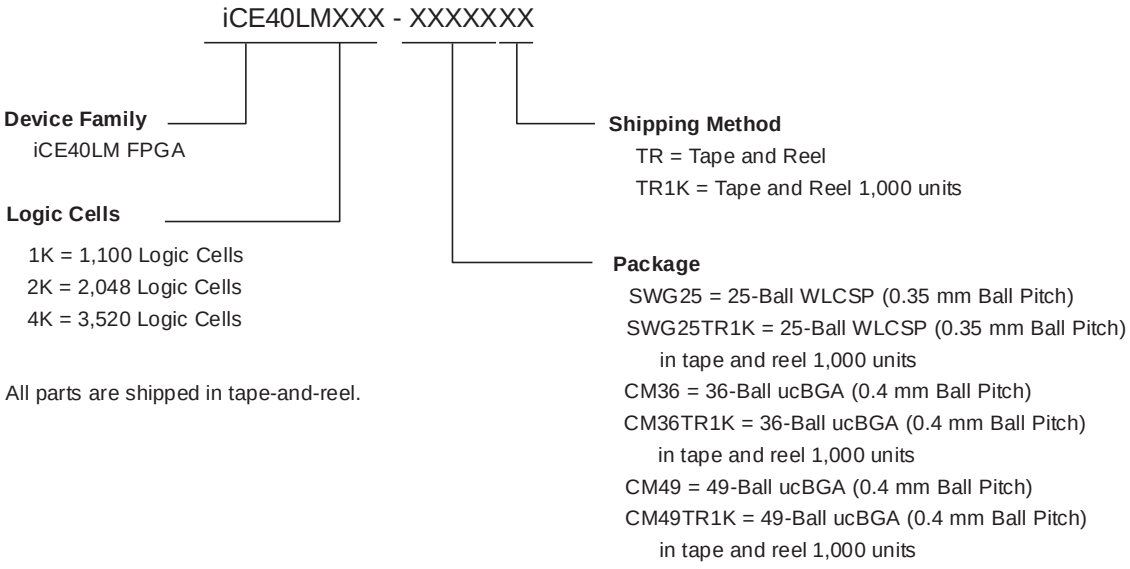
Signal Name	Function	I/O	Description
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location).
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location) [HD]=High Drive I/O.

5.2. Pin Information Summary

Pin Type		iCE40LM1K			iCE40LM2K			iCE40LM4K		
		SWG25	CM36	CM49	SWG25	CM36	CM49	SWG25	CM36	CM49
General Purpose I/O Per Bank	Bank 0	7	15	20	7	15	20	7	15	20
	Bank 2*	11	13	17	11	13	17	11	13	17
Total General Purpose I/Os		18	28	37	18	28	37	18	28	37
V_{CC}										
V_{CCIO}	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V_{CC_SPI}		0	0	1	0	0	1	0	0	1
V_{CCPLL}		0	1	1	0	1	1	0	1	1
Miscellaneous Dedicated Pins		2	2	2	2	2	2	2	2	2
GND		2	2	4	2	2	4	2	2	4
NC		0	0	0	0	0	0	0	0	0
Reserved		0	0	0	0	0	0	0	0	0
Total Balls		25	36	49	25	36	49	25	36	49
SPI Interfaces	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 2	1	1	1	2	2	2	2	2	2
I^2C Interfaces	Bank 0	1	1	1	2	2	2	2	2	2
	Bank 2	0	0	0	0	0	0	0	0	0

***Note:** Including General Purpose I/Os powered by V_{CC_SPI} and V_{CCPLL}.

5.3. iCE40LM Part Number Description



5.4. Ordering Part Numbers

5.4.1. Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temperature
iCE40LM1K-SWG25TR	1100	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM1K-SWG25TR1K	1100	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM1K-CM36TR	1100	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM1K-CM36TR1K	1100	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM1K-CM49TR	1100	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM1K-CM49TR1K	1100	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM2K-SWG25TR	2048	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM2K-SWG25TR1K	2048	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM2K-CM36TR	2048	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM2K-CM36TR1K	2048	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM2K-CM49TR	2048	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM2K-CM49TR1K	2048	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM4K-SWG25TR	3520	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM4K-SWG25TR1K	3520	1.2 V	Halogen-Free caBGA	25	IND
iCE40LM4K-CM36TR	3520	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM4K-CM36TR1K	3520	1.2 V	Halogen-Free ucBGA	36	IND
iCE40LM4K-CM49TR	3520	1.2 V	Halogen-Free ucBGA	49	IND
iCE40LM4K-CM49TR1K	3520	1.2 V	Halogen-Free ucBGA	49	IND

Supplemental Information

For Further Information

A variety of technical documents for the iCE40LM family are available on the Lattice web site.

- iCE40 Programming and Configuration (FPGA-TN-02001)
- iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02010)
- iCE40LM On-Chip Strobe Generator Usage Guide (FPGA-TN-02212)
- Advanced iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02011)
- Memory Usage Guide for iCE40 Devices (FPGA-TN-02002)
- iCE40 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02009)
- iCE40LM Pinout Files
- iCE40LM Pin Migration Files
- Thermal Management
- Lattice design tools
- Schematic Symbols

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Revision 1.9, July 2022

Section	Change Summary
Product Family	Updated the I/O counts in table Table 2.1.

Revision 1.8, February 2020

Section	Change Summary
Disclaimers	Added this section.

Revision 1.7, September 2018

Section	Change Summary
All	• Changed document number from DS1045 to FPGA-DS-02043. • Updated document template. • Added Acronyms in this document.
DC and Switching Characteristics	Updated sysCONFIG Port Timing Specifications section. Changed SPI_XCK to SPI_SCK.
Pinout Information	Updated Signal Descriptions section. Changed SPI_SDO to SPI_SO and SPI_SS_B to SPI_SS in Configuration SPI Pins.
Revision History	Updated revision history table to new template.

Revision 1.6, March 2016

Section	Change Summary
Architecture	Updated Typical I/O Behavior During Power-up section. Indicated 36-pin ucBGA in package in description.
DC and Switching Characteristics	Updated Recommended Operating Conditions 1 section. Revised foot-note 5.
Pinout Information	Updated Signal Description section. General update of signal names and descriptions.

Revision 1.5, March 2015

Section	Change Summary
DC and Switching Characteristics.	Updated sysI/O Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 V_{OH} Min. (V) from 0.5 to 0.4.

Revision 1.4, August 2014

Section	Change Summary
DC and Switching Characteristics.	• Updated the Recommended Operating Conditions section. Added V_{CC} and V_{CCPLL} information to footnote 1. • Updated Power Up Sequence section. Revised and added information on required power up sequence.

Revision 1.3, March 2014

Section	Change Summary
Ordering Information	Updated Ordering Part Numbers section. Changed packages from csBGA to ucBGA.

Revision 1.2, March 2014

Section	Change Summary
Architecture	• Updated Typical I/O Behavior During Power-up section. Added V_{CCIO_0} to the first statement. • Updated Power On Reset section. Added V_{CCIO_0} to the first statement.
Ordering Information	• Updated iCE40LM Part Number Description section. Added shipping method and packages. • Added part numbers in Ordering Part Numbers section.

Revision 1.1, January 2014

Section	Change Summary
All	Updated document status from Advance.
Introduction	Updated device features.
DC and Switching Characteristics	Updated the following tables: • sysCLOCK PLL Timing – Preliminary • Supply Current • sysCONFIG Port Timing Specifications.
Pinout Information	Updated SPI and Config SPI Ports information in Signal Descriptions table.

Revision 1.0, October 2013

Section	Change Summary
All	General updates for product launch.
Pinout Information	Updated ball map to 25-pin WLCSP.

Revision 00.2 EAP, September 2013

Section	Change Summary
All	General update to all sections.

Revision 00.1 EAP, August 2013

Section	Change Summary
All	Initial release

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